REMARKS

Applicant respectfully requests reconsideration of the present U.S. patent application. Claims 1-17 and 19-21 stand rejected under 35 U.S.C. § 103. No claims have been amended, canceled or added. Therefore, claims 1-17 and 19-22 remain pending.

Claim Rejections - 35 U.S.C. § 103

Rejections of Claims 1, 6 and 11-16 based on *Taniguchi* and *Holt*

Claims 1, 6 and 11-16 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,162,756 issued to Taniguchi et al. (*Taniguchi*) in view of Electronic Circuits – Digital and Analog by Holt (*Holt*). For at least the reasons set forth below, Applicant submits that claims 1, 6 and 11-16 are not rendered obvious by *Taniguchi* in view of *Holt*.

Claim 1 recited the following:

> a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal;
> a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal;
> a second amplifier subsection configured to receive the delayed input signal, and in response, provide a first delayed output signal; ...

Claim 15 is a method claim, and recites similar limitations.

Taniguchi discloses a high frequency signal power divider/combiner. See Fig. 2; col. 3, lines 7-16 and 55-56. The power divider/combiner includes six transmission lines (L_1-L_6) having lengths of one-quarter of the wavelength of the frequency of the signal passing through the transmission lines. See Fig. 2; col. 3, lines 17-23 and 37-38. In addition, the power divider/combiner uses four high frequency amplifiers (FETs) to

amplify a high frequency input signal and obtain a high power, high frequency output signal. See Fig. 2; col. 3, lines 55-59; col. 9, lines 16-18.

Examiner notes that the first amplifier in *Taniguchi* receives a signal through transmission line L_3. See Office Action, page 2, lines 15-17. Moreover, according to the Examiner, transmission line L_4 of *Taniguchi* is "a first delay element that introduces a delay to the input signal and applies this to the input of a 'second' amplifier FET_2." See Office Action, page 2, lines 18-19.

As set forth above, transmission lines L_3 and L_4 in *Taniguchi* are both one-quarter wavelength transmission lines. Therefore, if Examiner believes transmission line L_4 is a delay element, then Examiner must believe that transmission line L_3 is a delay element. Consequently, based on Examiner's interpretation, *Taniguchi* discloses two FETs that are each receiving a delayed input signal. As a result, *Taniguchi* does not disclose a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal, and in response, provide a first delayed output signal, as recited in claims 1 and 15. Thus, *Taniguchi* fails to disclose at least one limitation of claims 1 and 15.

Examiner cites *Holt* for the proposition that it would have been obvious "to provide *Taniguchi* with a bias control circuit(s) that biases the first and second amplifiers such that linear operation is obtained for these amplifiers." See Office Action, page 3, lines 28-30. Examiner does not assert that *Holt* discloses a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a

delayed input signal, and a second amplifier subsection configured to receive the delayed input signal.

Therefore, regardless of whether Examiner is correct regarding *Holt*, *Holt* fails to cure the deficiencies of *Taniguchi* pointed out by Applicant. Thus, *Taniguchi* in view of *Holt* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 1 and 15 under 35 U.S.C. § 103.

Claims 6 and 11-14 depend from claim 1. Claim 16 depends from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 6, 11-14 and 16 are not rendered obvious by *Taniguchi* in view of *Holt* for at least the reasons set forth above.

Rejections of Claims 2, 4, 17 and 20 based on *Taniguchi*, *Holt* and *Cheng*

Claims 2, 4, 17 and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt*, and further in view of Cheng et al., U.S. Patent Application No. 2002/0190790 (*Cheng*). For at least the reasons set forth below, Applicant submits that claims 2, 4, 17 and 20 are not rendered obvious by *Taniguchi* in view of *Holt* and *Cheng*.

As explained above, *Taniguchi* in view of *Holt* fails to disclose a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal, as recited in claims 1 and 15.

Examiner cites *Cheung* with regard to selectively supplying bias voltages. See Office Action, page 4, lines 13-19. Examiner does not assert that *Cheng* discloses a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal. Therefore, regardless of whether Examiner is correct regarding *Cheung*, *Cheung* fails to cure the deficiencies of *Taniguchi* in view of *Holt* pointed out by Applicant. Thus, *Taniguchi* in view of *Holt* and *Cheung* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Cheung* for at least the reasons set forth above.

As a result, *Cheng* fails to cure the deficiencies of *Taniguchi* in view of *Holt*. Thus, *Taniguchi* in view of *Holt* and *Cheng* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Cheng* for at least the reasons set forth above.

Claims 2 and 4 depend from claim 1. Claims 17 and 20 depend from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 2, 4, 17 and 20 are not rendered obvious by *Taniguchi* in view of *Holt* and *Cheng* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 2, 4, 17 and 20 under 35 U.S.C. § 103.

Rejection of Claim 21 based on *Taniguchi*, *Holt*, *Cheng* and *Atwater*

Claim 21 was rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt* and *Cheng*, and further in view of U.S. Patent No. 4,189,732 issued to Atwater (*Atwater*). For at least the reasons set forth below, Applicant submits that claim 21 is not rendered obvious by *Taniguchi* in view of *Holt*, *Cheng* and *Atwater*.

As explained above, *Taniguchi* in view of *Holt* fails to disclose a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal, as recited in claims 1 and 15.

Examiner cites *Atwater* with regard to a power supply circuit. See Office Action, page 4, line 24 - page 5, line 14. Examiner does not assert that *Atwater* discloses a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal. Therefore, regardless of whether Examiner is correct regarding *Atwater*, *Atwater* fails to cure the deficiencies of *Taniguchi* in view of *Holt* pointed out by Applicant. Thus, *Taniguchi* in view of *Holt* and *Atwater* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Atwater* for at least the reasons set forth above.

As a result, *Atwater* fails to cure the deficiencies of *Taniguchi* in view of *Holt* and *Cheng*. Thus, *Taniguchi* in view of *Holt*, *Cheng* and *Atwater* fails to disclose at least one

limitation of claim 15. Consequently, claim 15 is not rendered obvious by *Taniguchi* in view of *Holt*, *Cheng* and *Atwater* for at least the reasons set forth above.

Claim 21 depends from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claim 21 is not rendered obvious by *Taniguchi* in view of *Holt, Cheng* and *Atwater* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 21 under 35 U.S.C. § 103.

Rejection of Claim 3 based on *Taniguchi*, *Holt*, and *Sevic*

Claim 3 was rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt*, and further in view of U.S. Patent No. 6,069,525 issued to Sevic et al. (*Sevic*). For at least the reasons set forth below, Applicant submits that claim 3 is not rendered obvious by *Taniguchi* in view of *Holt* and *Sevic*.

As explained above, *Taniguchi* in view of *Holt* fails to disclose a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal, as recited in claims 1 and 15.

Examiner cites *Sevic* with regard to controlling both bias voltage and power supply voltage in response to an analog level control signal. See Office Action, page 5, lines 19-27. Examiner does not assert that *Sevic* discloses a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed

input signal. Therefore, regardless of whether Examiner is correct regarding *Sevic*, *Sevic* fails to cure the deficiencies of *Taniguchi* in view of *Holt* pointed out by Applicant. Thus, *Taniguchi* in view of *Holt* and *Sevic* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Sevic* for at least the reasons set forth above.

As a result, *Sevic* fails to cure the deficiencies of *Taniguchi* in view of *Holt*. Thus, *Taniguchi* in view of *Holt* and *Sevic* fails to disclose at least one limitation of claim 1. Consequently, claim 1 is not rendered obvious by *Taniguchi* in view of *Holt* and *Sevic* for at least the reasons set forth above.

Claim 3 depends from claim 1. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claim 3 is not rendered obvious by *Taniguchi* in view of *Holt,* and *Sevic* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 3 under 35 U.S.C. § 103.

Rejections of Claims 5, 7-10 and 19 based on *Taniguchi*, *Holt* and *Atwater*

Claims 5, 7-10 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt*, and further in view of *Atwater*. For at least the reasons set forth below, Applicant submits that claims 5, 7-10 and 19 are not rendered obvious by *Taniguchi* in view of *Holt* and *Atwater*.

As explained above, *Taniguchi* in view of *Holt* fails to disclose a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby

creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal, as recited in claims 1 and 15.

Examiner cites *Atwater* with regard to a power supply circuit. See Office Action, page 6, lines 1-20. Examiner does not assert that *Atwater* discloses a first amplifier subsection configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, and a second amplifier subsection configured to receive the delayed input signal. Therefore, regardless of whether Examiner is correct regarding *Atwater*, *Atwater* fails to cure the deficiencies of *Taniguchi* in view of *Holt* pointed out by Applicant. Thus, *Taniguchi* in view of *Holt* and *Atwater* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Atwater* for at least the reasons set forth above.

As a result, *Atwater* fails to cure the deficiencies of *Taniguchi* in view of *Holt*. Thus, *Taniguchi* in view of *Holt* and *Atwater* fails to disclose at least one limitation of claims 1 and 15. Consequently, claims 1 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Atwater* for at least the reasons set forth above.

Claims 5 and 7-10 depend from claim 1. Claim 19 depends from claim 15. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 5, 7-10 and 19 are not rendered obvious by *Taniguchi* in view of *Holt, Cheng* and *Atwater* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claims 5, 7-10 and 19 under 35 U.S.C. § 103.

Applicant would also like to address the Examiner's contention that "it appears that applicant is in full agreement with the Examiner" regarding the equivalence of FETs

and bipolars, and a non-linear mode of operation being desirable for saving energy, because Applicant did not make specific arguments regarding these points. See Office Action, page 7, line 26 – page 8, line 2. Please note that Applicant has argued that for at least the reasons set forth in this response, the cited references fail to disclose at least one limitation of the claims. Therefore, Applicant's failure to make arguments with regard to other issues raised by the Examiner does not mean that Applicant agrees with the Examiner, but means only that regardless of whether the Examiner is correct regarding those other issues, the references are deficient for at least the reasons given by the Applicant in this response.

CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections have been overcome. Therefore, claims 1-17 and 19-21 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the application.

Respectfully submitted,

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